

a.9
sensor indicates a temperature change that reduces the layer spacing in the antiferroelectric liquid crystal.

In the above method of driving an antiferroelectric liquid crystal panel, the layer structure controlling voltage waveform is output, for said optional length of time, at predetermined intervals of time.

IN THE CLAIMS:

Cancel claims 1-10 and substitute therefore the following new claims:

- sub B
a 10
- sub C
11. An antiferroelectric liquid crystal panel, having an antiferroelectric liquid crystal between a pair of substrates, which comprises a driving circuit adapted to output a layer structure controlling voltage waveform having a frequency of 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, for an optional length of time.
 12. An antiferroelectric liquid crystal panel, as claimed in claim 11, wherein said optional length of time is equal to the overall period of one frame.
 13. An antiferroelectric liquid crystal panel, as claimed in claim 11, wherein said optional length of time is equal to the period of one frame excluding a reset period.
 14. An antiferroelectric liquid crystal panel, as claimed in claim 11, wherein the pair of substrates are provided with scanning electrodes and signal electrodes, and wherein the panel comprises a control circuit which outputs the layer structure controlling voltage waveform to the scanning electrodes.
 15. An antiferroelectric liquid crystal panel, as claimed in claim 11, comprising a temperature sensor and a control circuit which outputs the layer structure controlling voltage waveform in accordance with information from the temperature sensor.

LAW OFFICES

FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000

a10

16. An antiferroelectric liquid crystal panel, as claimed in claim 11, comprising a control circuit which outputs the layer structure controlling voltage waveform, when the information from the temperature sensor indicates a temperature change that reduces the layer spacing in the antiferroelectric liquid crystal.

17. An antiferroelectric liquid crystal panel, as claimed in claim 11, comprising a control circuit which outputs the layer structure controlling voltage waveform, for said optional length of time, at predetermined intervals of time.

Sub B2

18. A method of driving an antiferroelectric liquid crystal panel having an antiferroelectric liquid crystal between a pair of substrates wherein a layer structure controlling voltage waveform having a frequency 1 Hz to 100 Hz and a voltage in the range of +10 V to +50 V or -10 V to -50 V, is output for an optional length of time.

Sub C

19. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein said optional length of time is equal to the overall period of one frame.

20. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein said optional length of time is equal to the period of one frame excluding a reset period.

21. A method of driving an antiferroelectric liquid crystal panel, as claimed in claim 18, wherein the pair of substrates are provided with scanning electrodes and signal electrodes, and wherein the layer structure controlling voltage waveform is output to the scanning electrodes

22. A method for driving an antiferroelectric liquid crystal panel as claimed in claim 18, wherein the antiferroelectric liquid crystal panel comprises a temperature